CLAIM COMPARISON

1. (Twice Amended) A memory cell comprising:

a trench capacitor formed in a substrate;

a shallow transistor trench (STT) formed in the substrate;

a transistor comprising:

a first diffusion region, the first diffusion region couples the capacitor to a gate of the transistor;

a second diffusion region, the second diffusion region couples the transistor to a bit line;

wherein the gate serves as a word line;

wherein the gate includes a buried portion and a non-buried portion, wherein the buried portion of the gate occupies the shallow transistor trench;

a gate dielectric having portions lining the shallow transistor trench; and

wherein one side of the gate dielectric is in contact with the buried portion of the gate and an opposite side of the gate dielectric is in contact with the first diffusion region.